In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

1. (Previously presented) A microprocessor comprising:

a processing unit;

a memory comprising a lower memory area and an extended memory area;

an address bus connecting said processing unit to said memory, and comprising a lower address bus for accessing said lower memory area, and an extended address bus for accessing said extended memory area;

means for executing instructions of an instruction set executable by said microprocessor, the instruction set comprising instructions for accessing said memory, a first instruction group comprising instructions for accessing said lower memory area, and a second instruction group distinct from the first instruction group and only comprising all the instructions for accessing said extended memory area; and

means for forcing to zero an extended address transmitted by said extended address bus when executing an instruction in the first instruction group so that said lower memory area is accessed.

2. (Previously presented) A microprocessor according to Claim 1, wherein each location in said memory is associated with a respective access address; the microprocessor further

comprising means for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing an instruction in the first instruction group.

3. (Previously presented) A microprocessor according to Claim 1, further comprising at least one internal register; and wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said memory; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

4. (Previously presented) A microprocessor according to Claim 1, wherein each location in said memory is associated with a respective access address; and for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area, the microprocessor further comprising means for maintaining an address of a jump destination location so that it points to a location in said lower memory area.

5. (Previously presented) A microprocessor according to Claim 1, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area; the microprocessor further comprising means for forcing an address and a value of a pointer that specifies access in the indirect mode so that the

pointer is located in said lower memory area and points to this area.

6. (Original) A microprocessor according to Claim 1, wherein the second instruction group comprises instructions for accessing said extended memory area in an indirect addressing mode.

7. (Original) A microprrccessor according to Claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area.

8. (Original) A microprocessor according to Claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area.

9. (Previously presented) A microprocessor according to Claim 1, further comprising a program pointer register having a size corresponding to a size of said address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in said memory.

10. (Original) A microprocessor according to Claim 1, wherein said lower memory area is accessible over 16 bits and said extended memory area is accessible over 24 bits.

11. (Previously presented) A microprocessor comprising:

a processing unit;

a memory comprising a lower memory area and an extended memory area;

an address bus connecting said processing unit to said memory, and comprising a lower address bus for accessing said lower memory area, and an extended address bus for accessing said extended memory area;

a set of instructions executable by said processing unit, the set of instructions comprising

a first instruction group comprising instructions for accessing said lower memory area, and

a second instruction group distinct from the first instruction group and only comprising all the instructions for accessing said extended memory area; and

a circuit for forcing to zero an extended address transmitted by said extended address bus when executing an instruction in the first instruction group so that said lower memory area is accessed.

12. (Previously presented) A microprocessor according to Claim 11, wherein each location in said memory is associated with a respective access address; the microprocessor further comprising means for forcing an access

address of a location to be accessed to point to a location in said lower memory area when executing an instruction in the first instruction group.

13. (Previously presented) A microprocessor according to Claim 11, further comprising at least one internal register; and wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said memory; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

14. (Previously presented) A microprocessor according to Claim 11, wherein each location in said memory is associated with a respective access address; and for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area, said instruction set further comprises instructions for maintaining an address of a jump destination location so that it points to a location in said lower memory area.

15. (Original) A microprocessor according to Claim 11, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area; and wherein said instruction set further comprises instructions for forcing an address and a value of a pointer that specifies access in the indirect mode so that the

pointer is located in said lower memory area and points to this area.

16. (Original) A microprocessor according to Claim 11, wherein the second instruction group comprises instructions for accessing said extended memory area in an indirect addressing mode.

17. (Original) A microprocessor according to Claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area.

18. (Original) A microprocessor according to Claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area.

19. (Previously presented) A microprocessor according to Claim 11, further comprising a program pointer register having a size corresponding to a size of said address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in said memory.

20. (Original) A microprocessor according to Claim 11, wherein said lower memory area is accessible over 16 bits and said extended memory area is accessible over 24 bits.

21. (Previously presented) A method for accessing a memory used by a microprocessor, the memory comprising a lower memory area and an extended memory area, the microprocessor comprising a processing unit, an address bus for connecting the processing unit to the memory and comprising a lower address bus for accessing the lower memory area and an extended address bus for accessing the extended memory area, the method comprising:

executing an instruction for accessing the lower memory area, the instruction belonging to an instruction set comprising a first instruction group comprising instructions for accessing the lower memory area, and a second instruction group distinct from the first instruction group and only comprising all the instructions for accessing the extended memory area; and

forcing to zero an extended address transmitted by said extended address bus when executing an instruction in the first instruction group so that said lower memory area is accessed.

22. (Previously presented) A method according to Claim 21, wherein each location in the memory is associated with a respective access address; the method further comprising forcing an access address of a location to be accessed to point to a location in the lower memory area when executing an instruction in the first instruction group.

23. (Previously presented) A method according to Claim 21, wherein the microprocessor further comprises at least one internal register; and wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in the memory; and

data transfer instructions between the arbitrary memory location and the at least one internal register.

24. (Previously presented) A method according to Claim 21, wherein each location in the memory is associated with a respective access address; and for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in the lower memory area; the method comprising maintaining an address of a jump destination location so that it points to a location in the lower memory area.

25. (Previously presented) A method according to Claim 21, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in the lower memory area; the method further comprising forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in the lower memory area and points to this area.

26. (Original) A method according to Claim 21, wherein the second instruction group comprises instructions

for accessing the extended memory area in an indirect addressing mode.

27. (Original) A method according to Claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located in the lower memory area.

28. (Original) A method according to Claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located within the extended memory area.

29. (Previously presented) A method according to Claim 21, wherein the microprocessor further comprises a program pointer register having a size corresponding to a size of the address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in the memory.

30. (Original) A method according to Claim 21, wherein the lower memory area is accessible over 16 bits and the extended memory area is accessible over 24 bit.